UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,206	07/20/2001	Michael Beuten	10191/1873	2708

26646	7590	05/06/2005

KENYON & KENYON
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER
RAMPURIA, SATISH

ART UNIT	PAPER NUMBER
2191	

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

<table>
<tr><td rowspan="3">Office Action Summary</td><td>Application No.</td><td colspan="2">Applicant(s)</td></tr>
<tr><td>09/910,206</td><td colspan="2">BEUTEN ET AL.</td></tr>
<tr><td>Examiner</td><td>Art Unit</td><td></td></tr>
<tr><td></td><td>Satish S. Rampuria</td><td>2191</td><td></td></tr>
</table>

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☒ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Response to Amendment

1. This action is in response to the after final amendment received on 04/14/2005.

2. The finality of the office action mailed on 11/29/2004 is withdrawn due to the rejection
    given under 35 U.S.C. 101 to claims 1-9 was not in the first office action mailed on
    04/21/2004.

3. The rejection under 35 U.S.C. 101 to claims 1-9 is withdrawn in view of applicant's
    amendment. Further, it is suggested that for claims 2-9 instead of "program" it should be
    "method" as previously presented.

4. Claims 1-9 are amended due to 35 U.S.C. 101 issue.

5. Claims 1-13 are pending.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all
    obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this
title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a
whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said ·
subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 7, 8, 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over
    admitted prior art in view of US Patent No. 6502209 to Bengtsson et al., hereinafter
    called Bengtsson and further in view of US Patent No. 6,412,071 Hollander et al.,
    hereinafter called Hollander.

Per claims 1, 2, 3, 10, 13, and 14:

Admitted prior art discloses:

- A program stored in a computer readable medium, the program performing a method for

monitoring an execution of a program that is executable on at least one microprocessor of a

micro controller using a debug logic of the micro controller (Applicant's specification, page 2,

lines 12-15 "The debug logic is used during the development of the program that is executable

on the at least one microprocessor of the micro controller and is used for improvement of the

visibility of the processes running in the micro controller")

- causing the debug logic to trigger an exception upon access to a specific address range

during a program execution time (Applicant's specification, page 3, lines 1-2 "The debug logic

can, as a rule, trigger an exception, e.g., an interrupt" and Applicant's specification, page 2, line

18 "The debug logic can learn from the address bus which selected address range was accessed")

- causing the debug logic to execute an exception routine after the exception is triggered

during the program execution time (Applicant's specification, page 3, lines 23-25 "When access

to one of these addresses is attempted, an exception is triggered and an exception routine is

executed")

Admitted prior art does not explicitly disclose causing the at least one microprocessor to

configure the debug logic.

However, Bengtsson discloses in an analogous computer system the debug chip is

configured in DUT (device under test) (col. 4, lines 37-38 "debug chip 110C configured in

DUT").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time

the invention was made to incorporate the method of configuring the microprocessor or DUT to

debug logic as taught by Bengtsson in to the method of monitoring the program as taught in admitted prior art. The modification would be obvious because of one of ordinary skill in the art would be motivated configure the prior art microprocessor with debug logic to eliminate the excessive costs of the producing a special version chip for debugging purposes as suggested by Bengtsson (col. 2, lines 24-30).

Neither admitted prior art nor Bengtsson disclose the access to the specific address range includes illegal access to a storage area.

However, Hollander discloses in an analogous computer system access to the specific address range includes illegal access to a storage area (col. 2, lines 62-67 "... receiving a caller routine return address... memory device... determining whether the caller routine address is valid by comparing the caller routing address with an associated process stack address area").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method to access to the specific address range includes illegal access to a storage area as taught by Hollander in to the method of monitoring the program as taught in combination system by admitted prior art and Bengtsson. The modification would be obvious because of one of ordinary skill in the art would be motivated to access the illegal access to a storage area to detect and prevent unauthorized illegal access within a computer system as taught by Hollander (col. 2, lines 1-21).

Per claim 4:

The rejection of claim 1 is incorporated, and further, admitted prior art does not explicitly disclose resetting the micro controller, starting up the micro controller again, and initializing the program.

However, Bengtsson discloses in an analogous computer system the power-on-reset unit coupled to the debug bus (col. 4, lines 21-24 "debug bus 140 is coupled to all chips... power-on-reset interrupts... other asynchronous events"). It is obvious to use the power-on-reset to reset microconroller and/or initialize the program.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the power-on-reset as taught by Bengtsson in to the method of monitoring the program as taught in admitted prior art. The modification would be obvious because of one of ordinary skill in the art would be motivated reset the microcontroller or DUT to make the new changes in effect.

Per claim 7 and 8:

The rejection of claim 1 is incorporated, and further, admitted prior art discloses:

- *the debug logic monitors whether the program accesses a preselectable address range of a memory during the program execution time* (Applicant's specification, page 2, lines 18-21 "The debug logic can learn from the address bus which selected address range was accessed, from the data bus, which data is to be written into the selected address range or was read out of the selected address range, and, from the control bus, whether a write or read access is to be performed on the selected address range")

Per claim 11:

The rejection of claim 10 is incorporated, and further, admitted prior art discloses:

- the control element corresponds to one of a read-only memory and a flash memory

(Applicant's specification, page 2, lines 3-4 "internal control elements (e.g., a read-only memory

or a flash memory), and/or further components")

Per claim 12:

The rejection of claim 10 is incorporated, and further, admitted prior art discloses:

- the micro controller is arranged in a motor vehicle (Applicant's specification, page 2, lines 4-

5 "This type of micro controller is, for example, part of a controller for a motor vehicle")

8. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted

prior art, Bengtsson in view of US Patent No. 6,697,972 to Oshima et al., hereinafter

called Oshima.

Per claims 5 and 6:

Neither admitted prior art nor Bengtsson discloses storing a fault in the memory and storing

memory address.

However, Oshima discloses in an analogous computer system storing a fault in the

memory and storing memory address (col. 5, lines 1-6 "OS fault detection time 13 and an OS

fault recovery method 14 are stored with regard to a monitored subject ID 18 (address), and AP

monitor fault detection time 15 and an AP monitor fault recovery method 16 are stored with

regard to a monitored subject ID 20").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time

the invention was made to incorporate storing a fault in the memory and storing memory

address as taught by Oshima in corresponding to the combination system for monitoring the

·program as taught by admitted prior art and Bengtsson. The modification would be obvious

because of one of ordinary skill in the art would be motivated to store fault type and memory

address in the memory to start monitoring debugging where it left off as suggested by Oshima

(col. 1, lines 40-46).

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art,

Bengtsson in view of US Patent No. 6,535,811 to Rowland et al., hereinafter called

Rowland.

Per claim 9:

Neither admitted prior art nor Bengtsson discloses a code sequence of the program, swapped out

from a flash memory of the micro controller into a random access memory of the micro

controller, in the flash memory.

However, Rowland discloses in an analogous computer system a code sequence of the

program, swapped out from a flash memory of the micro controller into a random access

memory of the micro controller, in the flash memory (col. 5, lines 23-25 "memory holding

the executable code, typically some type of ROM, had to be swapped with a memory having the

new executable code "burned in."" and col. 5, lines 27-29 "flash memory 22 comprises a flash

EPROM. Thus, executable code for the microcontroller can be rewritten as necessary").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time

the invention was made to incorporate the method of swapping the code between memories as

taught by Rowland into the method of monitoring the program as taught by the combination

system of admitted prior art and Bengtsson. The modification would be obvious because of one

of ordinary skill in the art would be motivated to swap the code between flash and RAM

memories to read write the data control relationship during engine operation as suggested by

(col. 2, lines 5-9).

Response to Arguments

10. Applicant's arguments with respect to claims 1, 10, and 13 have been considered but they

  are not persuasive.

In the remarks, the applicant has argued that:

  (i)   Nothing in the background information discloses (or suggest) the features a debug

          logic triggering an exception upon access to a specific address range during a

          program execution time and executing an exception routine after the exception is

          triggered during the program execution time such that the access to the specific

          address range includes illegal access to a storage area, as provided for in the context

          of claims 1, 10 and 13, as presented.

  (ii)   Bengtsson reference does not disclose or even suggest the feature of a debug logic

          triggering upon access to a specific address range during a program execution time

          and execution an exception routine after the exception is triggered during the program

execution time such that access to the specific address range includes illegal access to a storage area, as provided for in the context of claims 1, 10 and 13, as presented.

(iii) Office Action conclusorily asserts that "it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of configuring the microprocessor or DUT to debug as taught by Bengtsson in to the method of monitoring the program as taught in admitted prior art."

Examiner's response:

(i) In response to applicant's argument regarding the background information does not disclose the features recited in claims 1, 10, and 13, applicant's background information clearly states (page 2, lines 12-15, page 3, lines 1-2, and page 3, lines 23-25) the features, a debug logic triggering an exception upon access to a specific address range during a program execution time and executing an exception routine after the exception is triggered during the program execution time such that the access to the specific address range includes illegal access to a storage area (see the rejection above). Applicant only makes general allegations and does not point out any errors in the rejection. Therefore, the rejection is proper and maintained herein.

(ii) In response to applicant's argument regarding Bengtsson reference does not disclose or even suggest the features recited in claims 1, 10, and 13. It is noted that the rejection clearly points out where the combination of admitted prior art, Bengtsson, and Hollander (see the rejection above) teach the claimed features and why it would have been obvious to combine their teachings. Applicant only makes general

allegations and does not point out any errors in the rejection. Rather, in response to

applicant's arguments against the references individually, one cannot show

nonobviousness by attacking references individually where the rejections are based

on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871

(CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Therefore, the rejection is proper and maintained herein.

(iii)   In response to applicant's argument that the examiner's conclusion of obviousness is

based upon improper hindsight reasoning, it must be recognized that any judgment on

obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning.

But so long as it takes into account only knowledge which was within the level of

ordinary skill at the time the claimed invention was made, and does not include

knowledge gleaned only from the applicant's disclosure, such a reconstruction is

proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). It is

noted that the rejection clearly points out where the combination of admitted prior art,

Bengtsson, and Hollander (see the rejection above, page 4) teach the claimed features

and why it would have been obvious to combine their teachings. Specifically, to reset

the microcontroller to have the new changes in effect is very well known in the

computer art that to have the new changes in effect one in the ordinary skill in the art

would initialize the device by resetting the power ON/OFF (see the rejection above).

Applicant only makes general allegations of improper hindsight reasoning and does

not point out any errors in the rejection. Therefore, the rejection is proper and

maintained herein.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**. The examiner can normally be reached on **8:30 am to 5:00 pm** Monday to Friday except every other Friday and federal holidays. Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: 571-272-2100**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Tuan Q. Dam** can be reached on **(571) 272-3695**. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satish S. Rampuria
Patent Examiner
Art Unit **2191**
04/27/2005

ANIL KHATRI
PRIMARY EXAMINER